

Curriculum Vitae

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J. Stephan S. M. Wong

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Personalialia:

Date of birth: October 20, 1973
Place of birth: *Paramaribo, Suriname*
Gender: Male
Nationality: *Dutch*
Marital status: Married

Current Position: Assistant professor in the Computer Engineering Laboratory, Department of Microelectronics and Computer Engineering, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology (TU Delft), The Netherlands.

Education:

PhD EE Dec 2002 **Delft University of Technology** (TU Delft),
Delft, The Netherlands
Major: **Computer Engineering**
PhD Thesis: “*Microcoded Reconfigurable Embedded Processor*”
Advisor: Prof. Dr. Stamatis Vassiliadis (IEEE Fellow)

M.S. EE June 1997 **Delft University of Technology** (TU Delft),
Delft, The Netherlands
Major: **Computer Architecture**
Minor: **Information Theory**
GPA 8.2/10 (top 5% of class)
Thesis: “*Simulation of the Clustered Torus*”
Advisor: Prof. Dr. Stamatis Vassiliadis (IEEE Fellow)

Teaching Experience:

January '03 to Present (EE Department, Delft University of Technology, **Assistant Professor**)

- I have been responsible for developing and teaching the following courses:
 - ‘Logic Design’ (1st year Electrical Engineering BSc)
 - ‘Digital Systems’ (2nd year Computer Science BSc)
 - ‘Computer Architecture’ (2nd year Physics BSc)
 - ‘Embedded Systems’ (3rd year Electrical Engineering BSc)
 - ‘System Design with HDLs’ (1st year Computer Engineering MSc)
 - ‘Computer Architecture (Special Topics)’ (2nd year Computer Engineering MSc)
 - ‘Mars Rover Project’ (Electrical Engineering for Constructing Sciences minor)
- I am currently guiding seven (7) PhD students.
- I am currently guiding four (4) MSc students.
- I have guided eighteen (18) MSc students.
- I have guided and completed one (1) PhD student.
- I have partially guided and completed one (1) PhD student.

Research Interests: Embedded Processors, Computer Architecture and Engineering, Chip Multiprocessors, Multithreading, Multimedia Processing and Processors, High-Performance Processing and Processors, Microprogramming, Reconfigurable Computing, Synthesis and Verification, Computer Design, Logic Design, Computer Aided Design, Parallel Processing, Interconnection Networks, Multimedia Benchmarking, Grid Computing, Collaborative and Distributed Computing.

Synopsis: Currently, I am working within two research themes in the Computer Engineering laboratory, faculty of Electrical Engineering, Mathematics, and Computer Science, Delft University of Technology, The Netherlands. Within the MOLEN research theme, I am working on the **micro-architecture** of the **MOLEN polymorphic processor** (*co-founder*). Within the ARACHNE research theme, I am working on **network processing, collaborative grid computing**. During my PhD studies, I have been involved in research in **computer architectures** and **parallel processors**. More specifically, my focus was on **architectural multimedia extensions** for all mainstream and currently available processors. In particular, I worked on identifying possible candidates suited for parallelization and acceleration in hardware. An additional focus of my research has been the **performance evaluation** of reconfiguration schemes for **reconfigurable hardware** intended to support **multimedia** operations. In this evaluation process, I worked with a **cycle-precise simulator** and modified it extensively to suit performance evaluation purposes. Furthermore, manually editing the **multimedia benchmark** code in order to support the reconfiguration schemes was part of the process. In this process, I have also been involved in the **implementation** phase of reconfigurable hardware by utilizing **synthesis** and **verification** software. Currently, I am working on a new computing paradigm that combines **modifiable firmware** (microcode) and reconfigurable hardware with hardwired hardware, such as general-purpose **superscalar processor** cores. For my Master thesis, I worked on simulation and development of routing algorithms for a network of parallel processors arranged in a ‘clustered torus’-topology. The simulation framework allowed existing routing algorithms to be tested and has led to new algorithms.

Memberships:

- IEEE Member
- Member of the ACM
- HIPEAC Member

Languages:

- **Dutch:** mother tongue.
- **English:** fluent.
- **Chinese:** can speak two dialects fluently: Cantonese and Hakka.

Professional Activities:

Chair of the Board of Studies Electrical Engineering at TU Delft (February 2008 till now)

Member of the Board of Examiners CE and ES MSc programmes at TU Delft (October 2006 till now)

Involvement in organizing conferences:

1. **SAMOS Workshop 2009** - General chair & Steering committee member
2. **SAMOS Workshop 2006** - General chair
3. **SAMOS Workshop 2008 and ARCS 2009** - Program chair
4. **ICS 2006** - Proceedings chair
5. **ASAP 2005, SAMOS 2006-2008, DTIS 2007, and FPL 2007** - Financial chair
6. **SAMOS 2005** - Publicity chair
7. **SAMOS2006-2008, ARC 2006-2009 and FPL 2007-2008** - PC member

Served as Referee For: Over 16 conferences (and counting...)

Project involvement:

- EU STREP FP6 : VISIONS
- Cyprus government grant - DDM
- NL STW: Artemisia
- EU IP FP6 : Hartes

Invited Talks:

- 2008: Cankaya University (Turkey)
- 2007: University of Cyprus (Cyprus)
- 2006: EMICRO (Brazil), University of Cyprus (Cyprus)

Publications:

Editorships

1. Proceedings of the SAMOS Workshop 2008
2. Journal of Systems Architecture (Volume 53, Issue 10, October 2007)
3. Proceedings of the Symposium: “The Future of Computing” (2007)
4. Proceedings of the SAMOS Workshop 2006

Journal and Book Publications

1. J.Y. Hur, S. Wong, T.P. Stefanov, “Design Trade-offs in Customized On-Chip Crossbar Schedulers”, in *Journal of Signal Processing* (on-line), September 2008.
2. J.Y. Hur, S. Wong, S. Vassiliadis, “Partially Reconfigurable Point-to-Point FPGA Interconnects”, in *International Journal of Electronics*, vol. 95, no. 7, pp. 725-742, July 2008.
3. K. Tatas, P. Trancoso, E. Evripidou, S. Wong, “Rapid Prototyping of the Data-Driven Chip-Multiprocessor (D2-CMP) using FPGAs”, in *Parallel Processing Letters*, vol. 18, issue 2, pp. 291-306, June 2008.
4. L. Mhamdi, M. Hamdi, C. Kachris, S. Wong, S. Vassiliadis, “High-performance Switching based on Buffered Crossbar Fabrics”, in *Computer Networks Journal*, vol. 50, no. 13, pp. 2271-2285, September 2006.
5. S. Vassiliadis, S. Wong, G. N. Gaydadjiev, K. Bertels, G.K. Kuzmanov, E. Moscu Panainte, “The Molen Polymorphic Processor”, in *IEEE Transactions on Computers*, vol. 53, issue 11, pp. 1363-1375, November 2004.
6. S. Wong, S. Vassiliadis, S. D. Cotofana, “Future Directions of Programmable and Reconfigurable Embedded Processors”, in *Domain-Specific Processors: Systems, Architectures, Modeling, and Simulation*, pp. 235-257, January 2004.
7. S. Vassiliadis, S. Wong, S. D. Cotofana, “Microcode Processing: Positioning and Directions”, in *IEEE Micro*, vol. 23, no. 4, pp. 21-30, July 2003.

Conference Proceedings (peer-reviewed)

1. S. Wong, T. van As, G. Brown, “ ρ -VEX: A Reconfigurable and Extensible Softcore VLIW Processor”, in *Proceedings of the International Conference on Field-Programmable Technology (ICFPT2008)*, (Taipei, Taiwan), December 2008.
2. M. Ahmadi, S. Wong, “A Memory-optimized Bloom Filter using an Additional Hashing Function”, in *Proceedings of the IEEE Globecom 2008 Symposium*, (New Orleans, USA), December 2008.
3. M. Ahmadi, S.A. Ostadzadeh, S. Wong, “Rule-set Database Inspection: Towards Data Utilization in Packet Processing”, in *Proceedings of the International Conferences on the Latest Advances in Networks*, (Toulouse, France), December 2008.
4. S. Wong, M. Ahmadi, “Reconfigurable Architectures in Collaborative Grid Computing: An Approach”, in *Proceedings of the Second International Conference on Networks for Grid Applications (GridNets2008)*, (Beijing, China), October 2008.

5. R. Choupani, S. Wong, M. Tolun, "Weighted Embedded Zero Tree for Scalable Video Compression", in *Proceedings of the International Conference on Image Processing, Computer Vision, and Pattern Recognition (ICCV2008)*, (Las Vegas, NV, USA), July 2008
6. R. Hassanpour, A. Shahbahrami, S. Wong, "Adaptive Gaussian Mixture Model for Skin Color Segmentation", in *Proceedings of World Academy of Science, Engineering and Technology*, pp. 1-6, (Vienna, Austria), July 2008.
7. R. Hassanpour, S. Wong, A. Shahbahrami, "Vision-based Hand Gesture Recognition for Human Computer Interaction: A Review", in *Proceedings of the IADIS International Conference on Interfaces and Human Computer Interaction 2008*, pp. 125-134, (Amsterdam, The Netherlands), July 2008.
8. M. Ahmadi, S. Wong, "An Approach for Optimal Bandwidth Allocation in Packet Processing systems", in *Proceedings of Sixth Annual IEEE/ACM conference on Communication Networks and Services Research (CNSR 2008)*, pp. 208-214, (Halifax, Canada), May 2008.
9. O.S. Dragomir, E. Moscu Panainte, K.L.M. Bertels, S. Wong, "Optimal Unroll Factor for Reconfigurable Architectures", in *Proceedings of the 4th International Workshop on Applied Reconfigurable Computing*, pp. 63-72, (London, UK), March 2008.
10. A. Shahbahrami, J.Y. Hur, B.H.H. Juurlink, S. Wong, "FPGA Implementation of Parallel Histogram Computation", in *Proceedings of the 2nd HiPEAC Workshop on Reconfigurable Computing*, pp. 63-72, (Gteborg, Sweden), January 2008.
11. M. Ahmadi, S. Wong, "Hashing Functions Performance in Packet Classification", in *Proceedings of International Conference on the Latest Advances in Networks (ICLAN-2007)*, pp. 127-132, (Paris, France), December 2007.
12. M. Ahmadi, S. Wong, "A Cache Architecture for Counting Bloom Filters", in *Proceedings of 15th IEEE International Conference on Networks (ICON2007)*, pp. 218-223, (Adelaide, Australia), November 2007.
13. M. Ahmadi, S. Wong, "A Performance Model for Network Processor Architectures in Packet Processing Systems", in *Proceedings of the 19th International Conference on Parallel and Distributed Computing and Systems (PDCS 2007)*, pp. 176-181, (Cambridge, Massachusetts, USA), November 2007.
14. S.D. Breijer, F. Duarte, S. Wong, "An OCM Based Shared Memory Controller For Virtex 4", in *Proceedings of the 17th International Conference on Field Programmable Logic and Applications (FPL07)*, (Amsterdam, The Netherlands), August 2007.
15. S. Vassiliadis, F. Duarte, S. Wong, "A Load/Store Unit for a memcpy Hardware Accelerator", in *Proceedings of the 17th International Conference on Field Programmable Logic and Applications (FPL07)*, pp. 692-696, (Amsterdam, The Netherlands), August 2007.
16. S.J. Raaijmakers, S. Wong, "Run-Time Partial Reconfiguration for Removal, Placement and Routing on the Virtex-II", in *Proceedings of the 17th International Conference on Field Programmable Logic and Applications (FPL07)*, (Amsterdam, The Netherlands), August 2007.
17. R. Guo, J. G. Delgado-Frias, S. Wong, "Cache Replacement Policies for IP Address Lookups", in *Proceedings of The Fifth IASTED International Conference on Circuits, Signals, and Systems*, pp. 70-75, (Banff, Alberta, Canada), July 2007.
18. J.Y. Hur, T. P. Stefanov, S. Wong, S. Vassiliadis, "Customizing Reconfigurable On-Chip Crossbar Scheduler", in *IEEE 18th International Conference on Application-specific Systems, Architectures and Processors (ASAP07)*, (Montreal, Alberta, Canada), July 2007.
19. F. Duarte, S. Wong, "A memcpy Hardware Accelerator Solution for Non Cache-line Aligned Copies", in *Proceedings of 18th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP07)*, In LNCS 4419, pp. 61-72, (Montral, Canada), July 2007.
20. J.Y. Hur, T. P. Stefanov, S. Wong, S. Vassiliadis, "Systematic Customization of On-Chip Crossbar Interconnects", in *Proceedings of international workshop on applied reconfigurable computing (ARC07)*, In LNCS 4419, pp. 61-72, (Rio de Janeiro, Brazil), March 2007.
21. J.Y. Hur, S. Wong, S. Vassiliadis, "Partially Reconfigurable Point-to-Point Interconnects in Virtex-II Pro FPGAs", in *Proceedings of international workshop on applied reconfigurable computing (ARC07)*, In LNCS 4419, pp. 49-60, (Rio de Janeiro, Brazil), March 2007.

22. M. Ahmadi, S. Wong, "Modified Collision Packet Classification Using Counting Bloom Filter In Tuple Space", in *Proceedings of the 25th IASTED International Conference on Parallel and Distributed Computing and Networks (PDCN 2007)*, pp. 70-76, (Innsbruck, Austria), February 2007.
23. S. Wong, F. Duarte, S. Vassiliadis, "A Hardware Cache memcopy Accelerator", in *Proceedings of IEEE International Conference on Field Programmable Technology (FPT06)*, pp. 141-147, (Bangkok, Thailand), December 2006.
24. J.C.B. de Mattos, S. Wong, L. Carro, "The Molen FemtoJava Engine", in *Proceedings of the 17th IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP2006)*, pp. 19-22, (USA), September 2006.
25. F. Duarte, S. Wong, "Profiling Bluetooth and Linux on the Xilinx Virtex II Pro", in *Proceedings of 9th Euromicro Conference on Digital System Design (DSD06)*, pp. 229-235, (Dubrovnik, Croatia), August 2006.
26. S. Vassiliadis, G.K. Kuzmanov, S. Wong, E. Moscu Panainte, G. N. Gaydadjiev, K.L.M. Bertels, D. Cheresiz, "PISC: Polymorphic Instruction Set Computers", in *Proceedings of the International Workshop on Applied Reconfigurable Computing (ARC2006)*, pp. 274-286, (Delft, The Netherlands), March 2006.
27. I. Sourdis, D.N. Pnevmatikatos, S. Wong, S. Vassiliadis, "A Reconfigurable Perfect-Hashing Scheme for Packet Inspection", in *Proceedings of the 15th international Conference on Field-Programmable Logic and Applications (FPL)*, pp. 644-647, (Tampere, Finland), August 2005.
28. S. Vassiliadis, S. Wong, G. N. Gaydadjiev, K. Bertels, "Polymorphic Processors: How to Expose Arbitrary Hardware Functionality to Programmers", in *IEE FPGA Developer's Forum*, (London, United Kingdom), October 2003, (**invited talk**).
29. S. Wong, B. Stougie, S. Cotofana, "Alternatives in FPGA-based SAD Implementations", in *the Proceedings of the 1st IEEE International Conference on Field-Programmable Technology (FPT2002)*, pp. 449-452, (Hong Kong SAR, China), December 2002.
30. S. Wong, S. Vassiliadis, S. Cotofana, "A Sum of Absolute Differences Implementation in FPGA Hardware", in *the Proceedings of the 28th EUROMICRO Conference*, pp. 183-188, (Dortmund, Germany), September 2002.
31. S. Wong, S. Vassiliadis, S. Cotofana, "Future Directions of (Programmable and Reconfigurable) Embedded Processors", in *the Proceedings of the SAMOS 2002 Second International Samos Workshop on Systems, Architectures, Modeling, and Simulation*, (Samos, Greece), July 2002.
32. S. Wong, S. Cotofana, "On Teaching Embedded Systems Design to Electrical Engineering Students", in *the Proceedings of 3rd International Conference on Information Communication Technologies in Education (ICICTE2002)*, pp. 505-515, (Samos, Greece), July 2002.
33. S. Vassiliadis, S. Wong, S. Cotofana, "The MOLEN $\mu\mu$ -coded Processor", in *the Proceedings of the 11th International Conference on Field-Programmable Logic and Applications (FPL), Springer-Verlag Lecture Notes in Computer Science (LNCS) Vol. 2147*, pp. 275-285, (Belfast, UK), August 2001.
34. S. Wong, S. Vassiliadis, S. Cotofana, "Microcoded Reconfigurable Embedded Processors: Current Developments", in *Embedded Processor Design Challenges: Systems, Architectures, Modeling, and Simulation - SAMOS, Springer-Verlag Lecture Notes in Computer Science (LNCS) Vol. 2268*, pp. 207-224, (Samos, Greece), July 2001.
35. S. Vassiliadis, S. Wong, S. Cotofana, "Network Processors: Issues and Perspectives", in *the Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA-2001)*, pp. 1827-1833, (Las Vegas, NV, USA), June 2001.
36. S. Cotofana, S. Wong, and S. Vassiliadis, "Embedded Processors: Characteristics and Trends" (**invited paper**), in *the Proceedings of the 2001 ASCI Conference*, (Heijen, The Netherlands), May 2001.
37. S. Wong, S. Cotofana, and S. Vassiliadis, "Coarse Reconfigurable Multimedia Unit Extension", in *the IEEE Proceedings of the 9th Euromicro Workshop on Parallel and Distributed Processing (PDP) 2001*, (Mondova, Italy), February 2001.
38. S. Vassiliadis, G. Kuzmanov, S. Wong, "MPEG-4 and the New Multimedia Architectural Challenges", in *the Proceedings of the 15th International Conference on Systems for Automation of Engineering and Research (SAER-2001)*, pp 24-32, (Sofia, Bulgaria), January 2001

39. S. Wong, S. Cotofana, and S. Vassiliadis, "Multimedia Enhanced General-Purpose Processors", in *the IEEE Proceedings of the International Conference on Multimedia and Expo*, pp 1-4, (New York City, NY, USA), July 2000.
40. S. Wong, S. Cotofana, and S. Vassiliadis, "General-Purpose Processor Huffman Encoding Extension", in *the IEEE Proceedings of the International Conference on Information Technology: Coding and Computing*, pp. 158-163, (Nevada, USA), March 2000.
41. S. Vassiliadis, E.A. Hakkennes, S. Wong and G.G. Pechaneck, "The Sum Absolute Difference Motion Estimation Accelerator" in *the Proceedings of the 24th Euromicro Conference*, pp. 559-566, (Vasteras, Sweden), August 1998.

Short Overview:

Absolute numbers:

Year	Journal articles	Conference papers	Editorship	PhD students	MSc students
2008	3	10	1	2	2
2007	0	12	2	0	5
2006	1	4	1	0	4
2005	0	1	0	0	1
2004	2	0	0	0	1
2003	1	1	0	0	4
2002	0	4	0	0	1
2001	0	6	0	0	0
2000	0	2	0	0	0
1999	0	0	0	0	0
1998	0	1	0	0	0
Total	6	41	4	2	18

"Publish or Perish" results (not complete due to incompleteness of Google Scholar):

Papers	Citations	Years	Cites/ year	Cites/ paper	Cites/ author	Papers/ author	Authors/ paper
36	376	9	41.78	10.44	101.51	11.60	3.31

h-index	g-index	hc-index	hI-index	hI,norm	AWCR	AW-index	AWCRpA
10	19	8	2.94	5	67.97	8.24	18.30