



# Stamatis Vassiliadis Symposium “The Future of Computing”

**Stamatis Vassiliadis Symposium 28 September, 2007**

On September 28 2007, the CE laboratory of Delft University of Technology, the Netherlands, is organizing a symposium to the honor of professor Stamatis Vassiliadis, chair of the CE laboratory, who regretfully passed away earlier this year. The theme of the symposium is : “*THE FUTURE OF COMPUTING*”. A number of distinguished colleagues and friends of *professor Vassiliadis*, will contribute to a book and will give a presentation at the symposium. The confirmed list of contributors is the following:

Wayne Luk	Imperial College	UK
Jose Duato	Polytechnic University of Valencia	Spain
Alex Orailoglu	University of California San Diego	USA
David Bernstein	IBM	Israel
Manolis Katevenis	Forth	Greece
Nikitas Dimopoulos	University of Victoria	Canada
Eric Schwarz	IBM	USA
Mateo Valero	Polytechnic University of Catalunya	Spain
Sudakhar Yalamanchili	Georgia Tech	USA
Yale Patt	University of Texas at Austin	USA
Michael Flynn	Stanford University	USA
Jim Smith	University of Wisconsin Madison	USA
Walid Najjar	University of California Riverside	USA
Reiner Hartenstein	TU Kaiserslautern	Germany
Per Stenström	Chalmers University	Sweden
Bart Blaner	IBM	USA

You are cordially invited to participate in this symposium and are encouraged to register at the following website before the **18<sup>th</sup> of September**:

<http://ce.et.tudelft.nl/symposium/>

**PARTICIPATION IS FREE BUT REGISTRATION IS MANDATORY.**

Computer Engineering group,  
Faculty of EEMCS,  
Delft University of Technology

*The symposium is financially supported by the ICT Delft Research Centre and the faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology*



# THE FUTURE OF COMPUTING

September 28 2007

13:30:00	Opening by the Rector Magnificus, Prof. Dr. Fokkema	
13:40:00	Peter Petrov, Alex Orailoglu	Customizable Embedded System Architectures
13:55:00	Per Stenström	The paradigm shift to Multi cores: opportunities and challenges
14:10:00	W. Najjar, B.Buyukkurt, Z.Guo, J. Villareal, J. Cortes, A. Mitra	Compiled code acceleration on FPGAs
14:25:00	M. Katevenis	Interprocessor communication seen as load-store instruction generalisation
14:40:00	W. Luk	Self-optimizing and self-verifying design: a vision
14:55:00	S. Yalamanchili, S.Ramaswamy, G. Diamos From Adaptive to self-tuned systems	
15:10:00	Break	
15:40:00	M. Flynn	Super SoC: putting the whole (autonomous) system on the chip (ASOC)
15:55:00	E. Schwarz	Future Research in computer arithmetic
16:10:00	J. Duato, F. Silla	High-performance interconnection networks: a key component in future systems
16:25:00	N. Agarwal, N. Dimopoulos	Optimal FSM partitioning for lowpower
16:40:00	R. Hartenstein	The Von Neumann Syndrome
16:55:00	Break	
17:25:00	D. Bernstein, B. Mendelson	Software Enablement for Multicore Architectures
17:40:00	Y. Patt	Microprocessor performance, phase 2 harnessing the transformation hierarchy
17:55:00	J. Smith	Future superscalar processors based on instruction compounding
18:10:00	M. Pireguas, M. Valero, R. Chavez, G. Gaydadjiev, S.Vassiliadis	Vectorized AES core for high throughput secure environments
18:25:00	M. Valero	A+A=A
18:30:00	Reception	
20:00:00	Closing	

**Location : Delft University of Technology, Conference Centre Aula - Room A, Mekelweg**

**Sponsored by : ICT Delft Research Centre and Faculty of Electrical Engineering, Mathematics and Computer Science and Hipeac Network of Excellence**