



# Data Communication and Memory Hierarchy in Heterogeneous Reconfigurable SoC

*(within the framework of EU project "MORPHEUS")*

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Fabio Campi



Data Communication & Memory Hierarchy...



## Outline

- About MORPHEUS
- MORPHEUS architecture
- Overview of its reconfigurable cores
- Memory structure
- PiCoGA address generator
- Results and future work

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## About MORPHEUS

Multipurpose Dynamically Reconfigurable Platform for Intensive Heterogeneous processing



|   |  |
|---|--|
| <b>Objectives:</b>  | <b>Applications:</b>   |
| <ul style="list-style-type: none"><li>• Faster time-to-market</li><li>• Increased flexibility</li><li>• Data intensive processing</li><li>• Power consumption (less mission critical)</li></ul> | <ul style="list-style-type: none"><li>• Broadband Wireless Access Systems</li><li>• Network Routing Systems</li><li>• Professional Video</li><li>• Homeland Security</li></ul> |

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## MORPHEUS Goal



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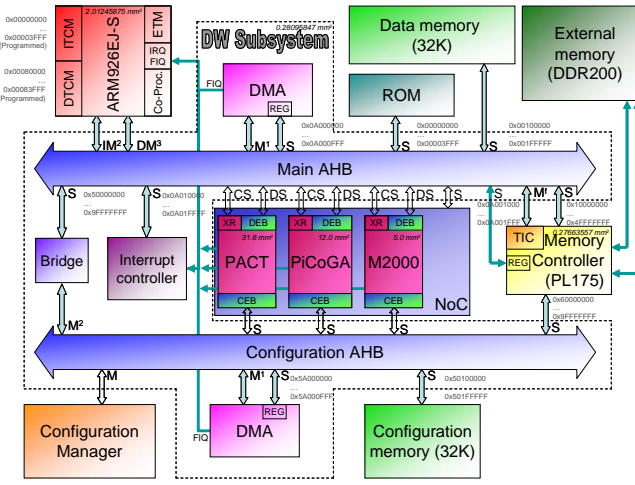
## Participant List

| Participant name                         | Participant short name | Country         |
|--|------------------------|-----------------|
| THALES Research & Technology             | TRT                    | France          |
| Deutsche Thomson-Brandt GmbH             | DTB                    | Germany         |
| Intracom SA Telecom Solutions            | Intracom               | Greece          |
| Lucent Technologies Network Systems GmbH | Lucent                 | Germany         |
| Thales Optronics SA                      | TOSA                   | France          |
| STMicroelectronics Srl                   | ST                     | Italy           |
| PACT GmbH                                | PACT                   | Germany         |
| M2000                                    | M2000                  | France          |
| Associated Compiler Experts bv           | ACE                    | The Netherlands |
| CriticalBlue                             | CBlue                  | United Kingdom  |
| Universität Karlsruhe                    | UK                     | Germany         |
| Technische Universiteit Delft            | TUD                    | The Netherlands |
| Commissariat à l'Énergie Atomique - LIST | CEA                    | France          |
| Université de Bretagne Occidentale       | UBO                    | France          |
| Universita di Bologna                    | ARCES                  | Italy           |
| ARTTIC                                   | ART                    | France          |

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## MORPHEUS Architecture

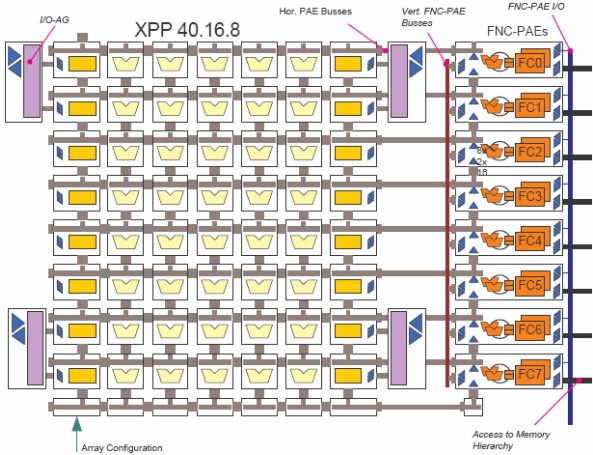


- 3 heterogeneous reconfigurable engines (HRE)
- Controlled by ARM9
- Dedicated configuration manager (CM)
- Separate AMBA busses
- NoC extends inter-HRE communication
- Data/configuration exchange buffers (DEB/CEB) bridge different clock domains
- Task triggering – according to Molen paradigm through exchange registers (XR)

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## Cores' overview: PACT XPP

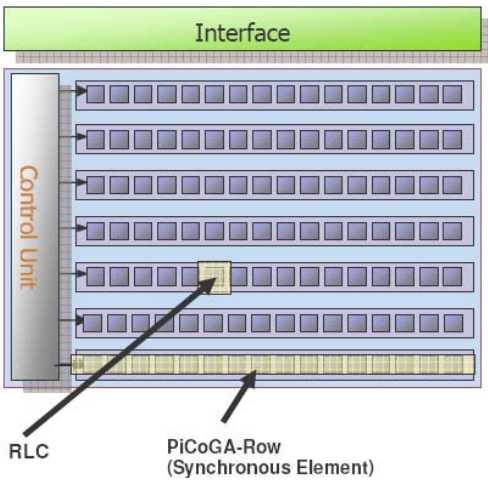


- Coarse-grain
- Intensive parallel processing
- Fast reconfiguration
- 2 categories of application:
  - Data-flow
  - Control-flow
- 3 types of configurable processing array elements (PAE)
  - ALU-PAE
  - RAM-PAE
  - FNC-PAE

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## Cores' overview: PiCoGA



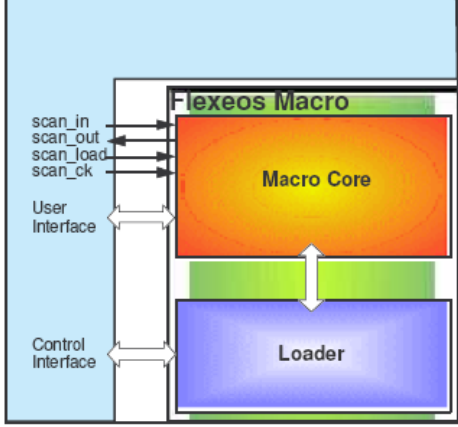
- Medium-grain
- Features instruction level parallelism (ILP)
- 16x24 array of reconfigurable logic cells (RLC)
- Each RLC includes:
  - 4-bit ALU
  - 64-bit LUT
- Pipelined data-flow graph (PDFG) support
- 4 configuration contexts
- Up to 4 PiCoGA-operations per contexts
- 12 inputs, 4 outputs with 32-bit width

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## Cores' overview: M2000

**SoC**





The diagram illustrates the SoC architecture. It features a central **Flexeos Macro** block containing a **Macro Core** and a **Loader**. The **Macro Core** is connected to a **User Interface**, and the **Loader** is connected to a **Control Interface**. The **Flexeos Macro** also has scan signals: **scan\_in**, **scan\_out**, **scan\_load**, and **scan\_ck**.

- Fine-grain eFPGA
- Macro core includes:
  - 4K Multi-Function logic Cells (MFC) combining:
    - 4 input LUT
    - D flip-flop
  - 8 dual-port RAM
  - 32 multiply/accumulate operators (MAC)
  - 128x8 bit adders
- Loader:
  - Loads the configuration stream
  - Simplifies silicon test

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## Communication Flows

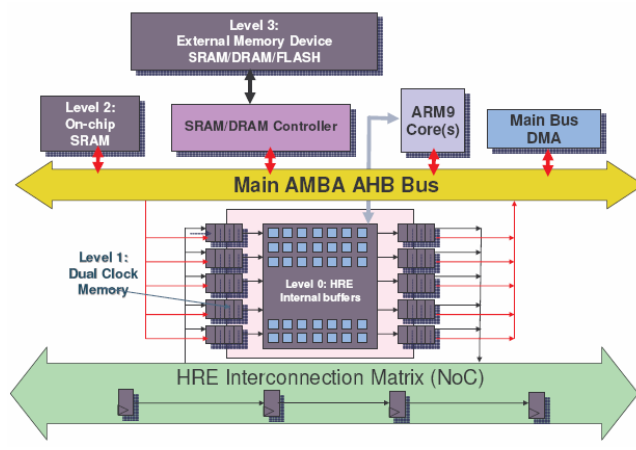
1. Computational data flow
  - Main processor
  - DMA(s)
  - I/O peripherals
  - Communication infrastructure
    - AMBA (main AHB)
    - NoC
2. Configuration data flow
  - Configuration Manager
  - DMA(s)
  - AMBA (configuration AHB)
3. Control flow
  - Main processor
  - AMBA (main AHB)
4. I/O interfaces
  - I/O resources
  - Communication infrastructure
    - AMBA (main & conf. AHB)
    - NoC (possibly)

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## System Level Data Storage



- AMBA
  - Low cost
  - Low performance
- NoC
  - High bandwidth
  - Streaming computational mode
- Memories:
  - Level 1 – 800Mb/s
  - Level 2 – 500Mb/s
  - Level 3 – 70Mb/s



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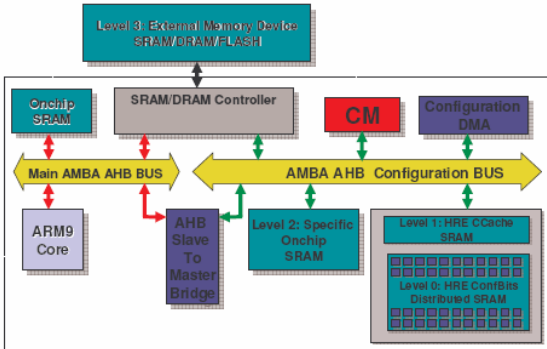
## Control Data Storage

- Issuing of configuration tasks and computation commands according to the Molen paradigm
- Synchronization of task dependencies
- Routing of data and transfers between architectural resources: programming of DMAs and NoC
- Synchronization of exclusive access to DEBs
- Programming of internal HRE address generators
- Configuration control: CM task synchronization, configuration DMA(s) programming

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## Configuration Data Storage



- Mastered by the configuration manager (CM)
- AHB-to-AHB bridge connection with the main bus
- NoC is NOT used
- Memory level 1: ping-pong buffering mechanism

| IP          | Config. size | Array size |
|-------------|--------------|------------|
| PACT XPP    | 16 KBytes    | 8x8        |
| PiCoGA      | 72 KBytes    | 4x(24x16)  |
| M2000 eFPGA | 60 KBytes    | 4K MFCs    |

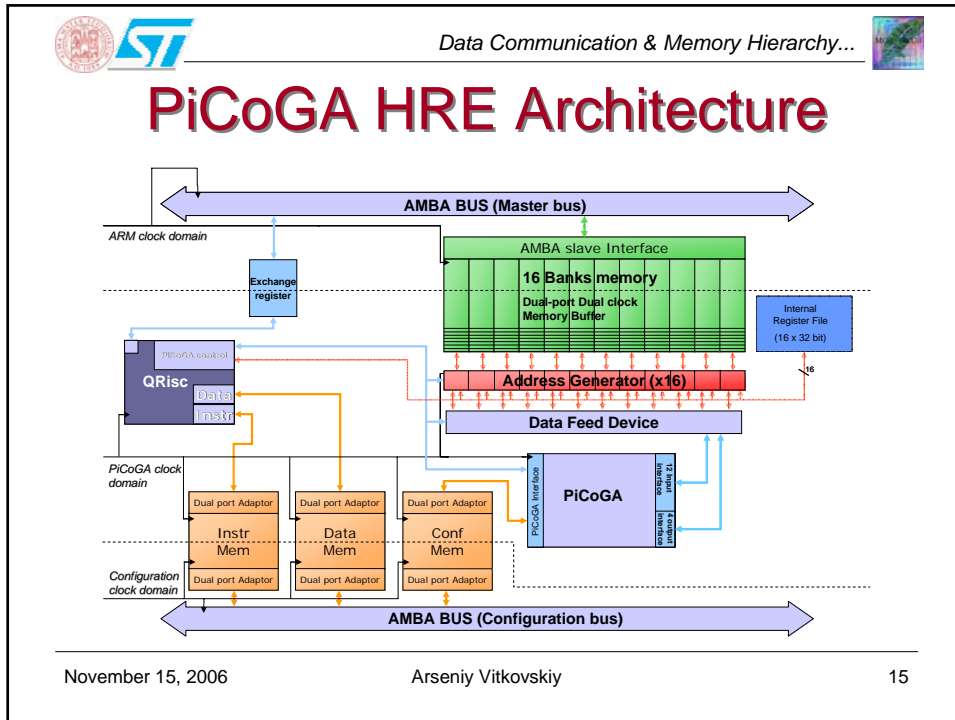
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## Summary

- 3 heterogeneous reconfigurable cores
- 4 clock domains bridged with local buffers (DEBs/CEBs)
- Separate busses for data/control and reconfiguration flows
- NoC for intensive data processing
- ARM9 controlled
- Tasks issuing according to the Molen paradigm

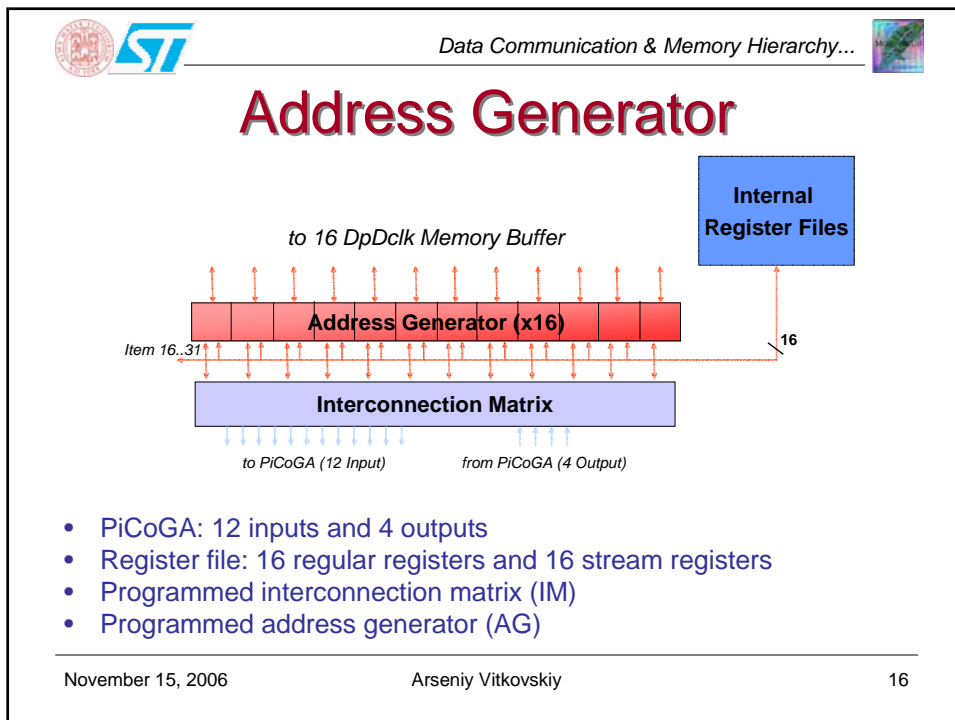
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## AG Programming Model

*Set\_DF(Item, Addr, Count, Mask, Stride, Step, rw)* where:

- *Item*: is an index value (range 16..31) that indicates the identifier for the right address generator
- *Addr*: is the base address inside the memory where the first access performs (range 0...4095)
- *Count*: number of data words inside a chunk (range 0...4095)
- *Mask*: size of the circular buffer (range  $2^0...2^{16}$ )
- *Stride*: distance between data chunks (range -127..+128)
- *Step*: data words accessing steps (range -127..+128)
- *rw*: Read/write access

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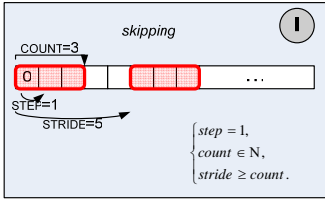
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## Possible Memory Accesses

Solid data chunks

skipping

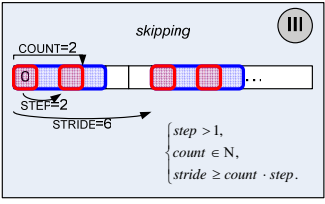


I

$$\left\{ \begin{array}{l} \text{step} = 1, \\ \text{count} \in \mathbb{N}, \\ \text{stride} \geq \text{count}. \end{array} \right.$$

Fragmented data chunks

skipping

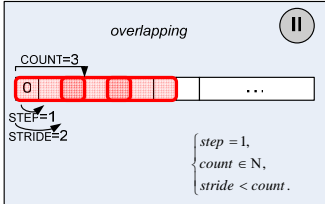


III

$$\left\{ \begin{array}{l} \text{step} > 1, \\ \text{count} \in \mathbb{N}, \\ \text{stride} \geq \text{count} \cdot \text{step}. \end{array} \right.$$

Solid data chunks

overlapping

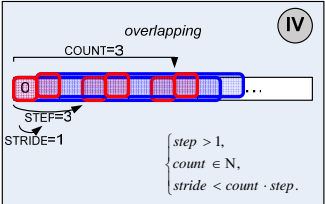


II

$$\left\{ \begin{array}{l} \text{step} = 1, \\ \text{count} \in \mathbb{N}, \\ \text{stride} < \text{count}. \end{array} \right.$$

Fragmented data chunks

overlapping





IV

$$\left\{ \begin{array}{l} \text{step} > 1, \\ \text{count} \in \mathbb{N}, \\ \text{stride} < \text{count} \cdot \text{step}. \end{array} \right.$$

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## Circular Buffer

```

Local_address = next_address;
Base_address = next_base_address;
address = (Base_address & ~mask) + (local_address & mask);
next_address = local_address + step;
next_base_address = (base_address + stride)
    if (Count == EndOfCount);
    
```

Example:



Base = 0x1; Step = 1; Stride = 4; count = 4; mask = 0b11;

Generated address sequence:

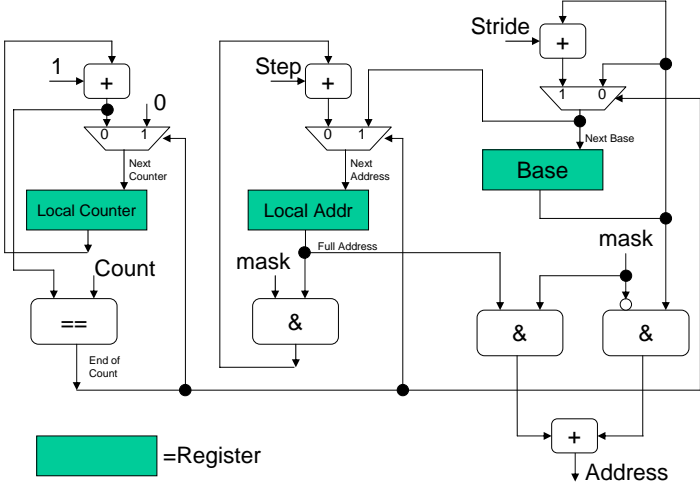
0x01 – 0x02 – 0x03 – 0x00 – 0x05 – 0x06 – 0x07 – 0x04 – 0x09 - ...

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## AG Block Diagram



   = Register

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## Previous Version Results

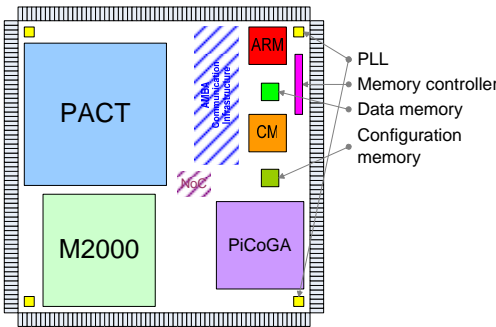
- VHDL implementation
- Synthesis with STM CMOS090 @ 200MHz
- Replacement of standard cells with memory modules (total area reduction by 2.2x)
- Power consumption decreased proportionally to the area reduction (+ traffic savings)
- “A Stream Register File Unit for Reconfigurable Processors”, ISCAS06

| DSPStone benchmark | Matrix1 | Matrix2 | FIR 2D |
|--------------------|---------|---------|--------|
| Traffic savings    | 81.8%   | 85.7%   | 68.1%  |
| Time savings       | 58.3%   | 62.9%   | 47.9%  |

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## Preliminary Results of Project




- Data communication and memory hierarchy definition
- PiCoGA address generator
- VHDL implementation
- Test and verification
- HW synthesis
  - CMOS90 @ 300MHz
  - 3.8 mm<sup>2</sup>
- Floor-plan (240-250 I/O pads)

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## Future Work


- Introduce reconfigurable IPs in the system
- Perform software simulations with SystemC model and application kernels from IP vendors
- Make system tuning according to the simulation results
- Testing and verification
- Continue hardware implementation

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## The End



Thank you!

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